REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claim 1 has been amended with respect to formal matters. Claim 7 has been amended, in the manner requested in the Office Action, to overcome the objection thereto.

Claims 1, 2, 4, 5, and 8 stand rejected, under 35 USC §103(a), as being unpatentable over Okamura (US 5,521,541) in view of Skergan et al. (US 6,452,435). Claim 3 stands rejected, under 35 USC §103(a), as being unpatentable over Okamura in view of Skergan and Godfrey et al. (US 6,550,031). Claims 6 and 9 stand rejected, under 35 USC §103(a), as being unpatentable over Okamura in view of Skergan and McElvain et al. (US 2006/0095872). Claim 7 stands rejected, under 35 USC §103(a), as being unpatentable over Okamura in view of Skergan and Meier et al. (US 6,854,567). The Applicants respectfully traverse these rejections.

An important feature of the invention of claim 1 is a scan clock circuit, for providing a scan clock to a plurality of flip-flop circuits which configure a scan chain, and a separate clock circuit for providing normal clocking operation of the flip-flop circuits. Another important feature is a lattice-shaped wiring portion for the scan clock circuit.

Arranging a lattice-shaped wiring portion for the scan clock circuit helps prevent the generation of a differential delay (i.e., clock skew) resulting from factors, such as manufacturing variation and delay calculation error, that may not be detected by simulation in a micro fabrication process. However, the power consumption for a lattice-shaped wiring portion is higher than that for a tree-structure wiring portion and the timing restriction of the clock circuit for normal operation, when data is shifted, is not as strict as that for the scan clock circuit. Therefore, to reduce power consumption, the clock circuit for normal operation may be configured in a tree structure.

Claim 1 recites two separate clock circuits, one configured with lattice-shape wiring for providing clock to a plurality of flip-flop circuits of a scan chain and another for normal clocking operation of the flip-flop circuits. With two separate clock circuits, the claimed invention may prevent the above-mentioned clock skew and a resulting malfunction of the circuit during a scan test.

Although the Office Action proposes that Okamura discloses a clock circuit having lattice-shaped wiring (see Office Action section 4, first sentence), the Office Action does not propose that Okamura discloses or suggests two clock circuits, as recited in claim 1. More specifically, the Office Action does not

propose that Okamura discloses the claimed features of one clock circuit configured with lattice-shape wiring for providing clock to a plurality of flip-flop circuits of a scan chain and another clock circuit for normal clocking operation of the flip-flop circuits.

Because Okamura's device lacks the above-noted features, Okamura's device cannot achieve the above-described advantages of the present claimed invention.

Skergan is cited in the Office Action for teaching the use of mesh wiring for a scanning clock circuit (see Office Action page 3, lines 3-6), and the Office Action proposes that Okamura's device may be modified, based on the teachings of Skergan, to use the lattice-shaped wiring of the clock circuit for both normal and scanning operations so as to reduce the complexity of the wiring (see Office Action section 4, last sentence). However, the proposed modification is not a feature of claim 1.

Instead, claim 1 recites two clock circuits, one clock circuit configured with lattice-shape wiring for providing clock to a plurality of flip-flop circuits of a scan chain and another clock circuit for normal clocking operation of the flip-flop circuits. The applied Okamura and Skergan references do not teach or suggest these features, alone or in combination, and the Office Action does not propose otherwise.

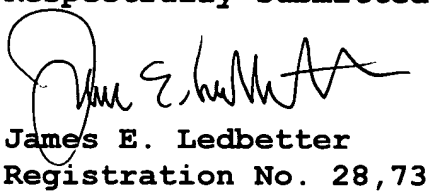
McElvain and Meier are not cited in the office action for any teaching of the above-noted subject matter of claim 1.

Accordingly, the Applicants respectfully submit that the prior art of record, considered individually or in combination, do not suggest the subject matter defined by claim 1 or the benefits derived therefrom. Therefore, the rejections applied to claims 3, 6, 7, and 9 are obviated and allowance of claim 1 and all claims dependent therefrom is warranted.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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